



REPLACEMENT SHEET

Title: METHOD FOR MEASURING THE DELAY
TIME OF A SIGNAL LINE

Applicant: Gregorius et al.
Serial No.: 10/808,143
Atty Docket: 1406/144/2

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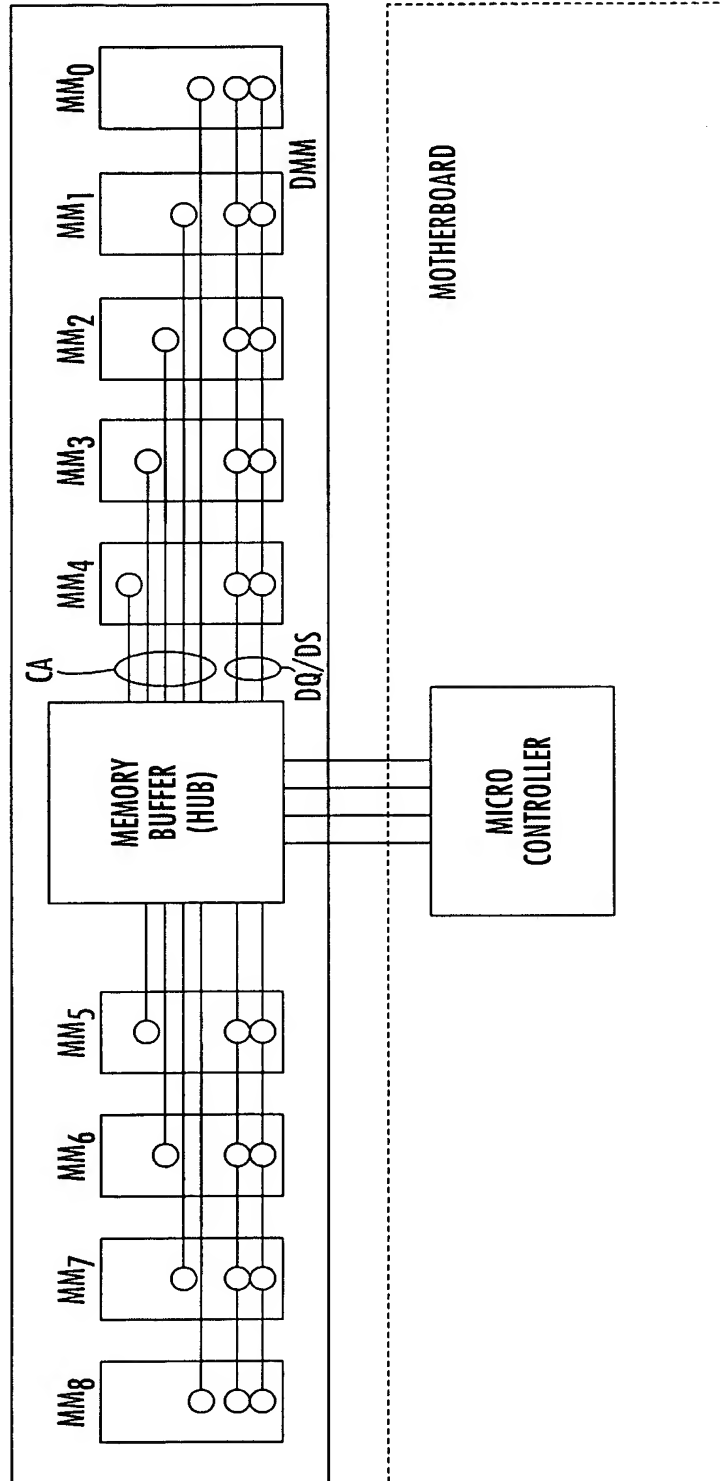


FIG. 1
(PRIOR ART)

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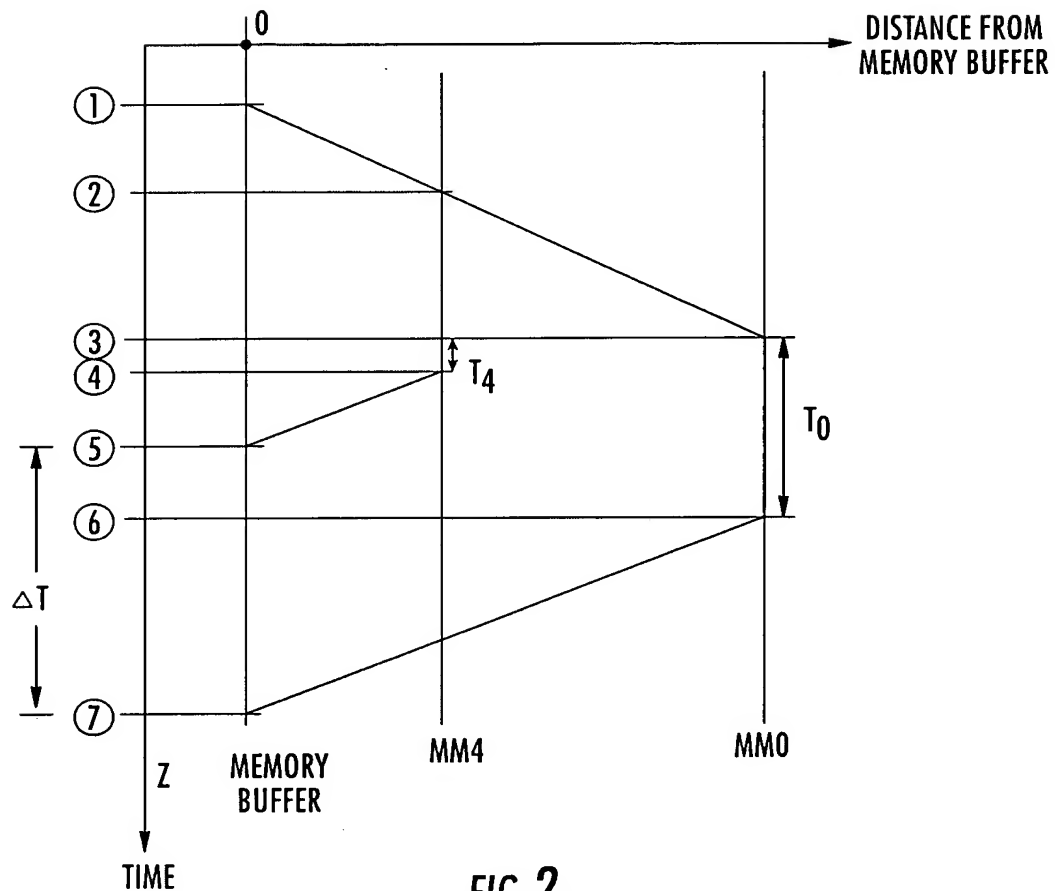
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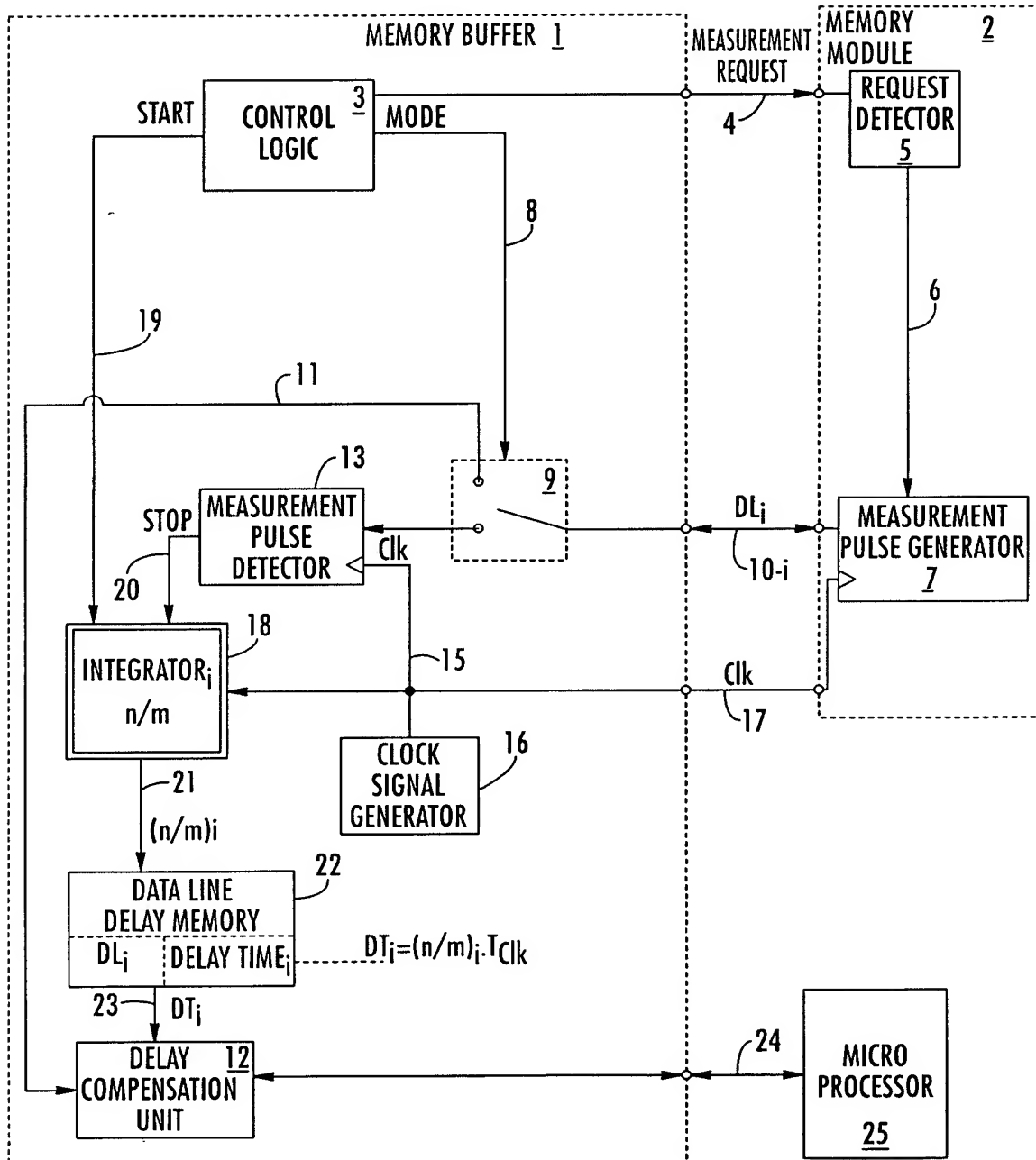


FIG. 3

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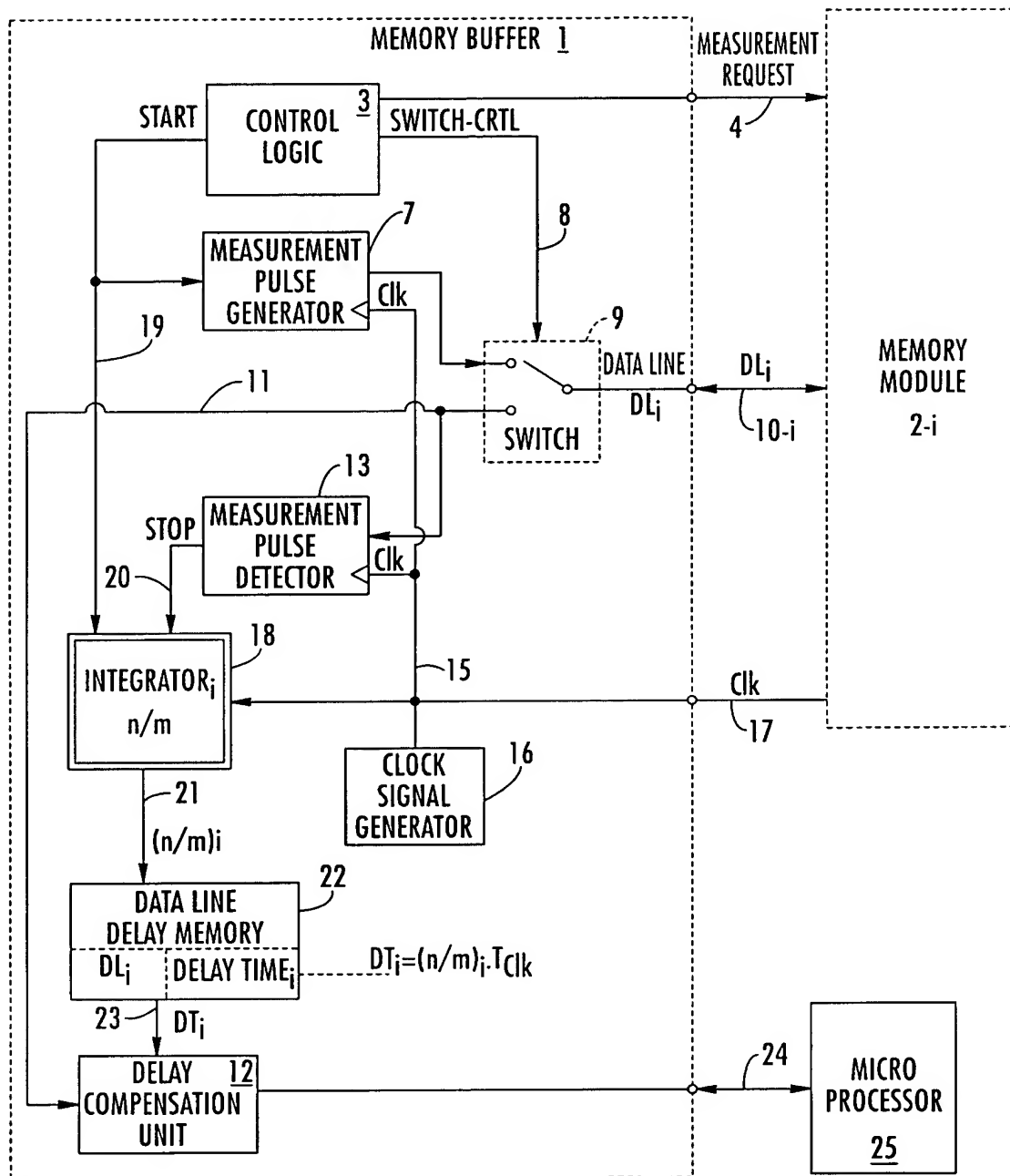


FIG. 4

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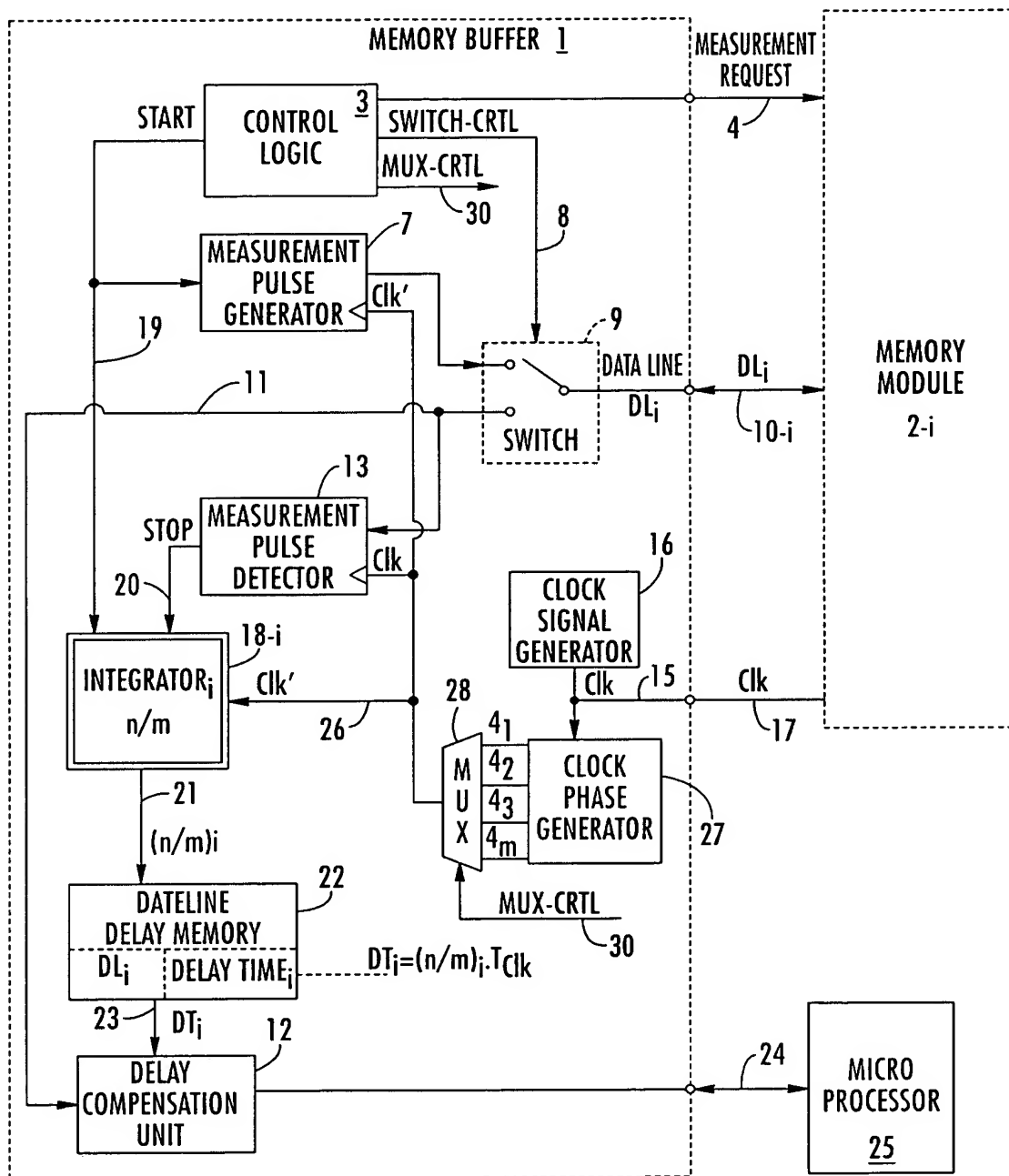


FIG. 5

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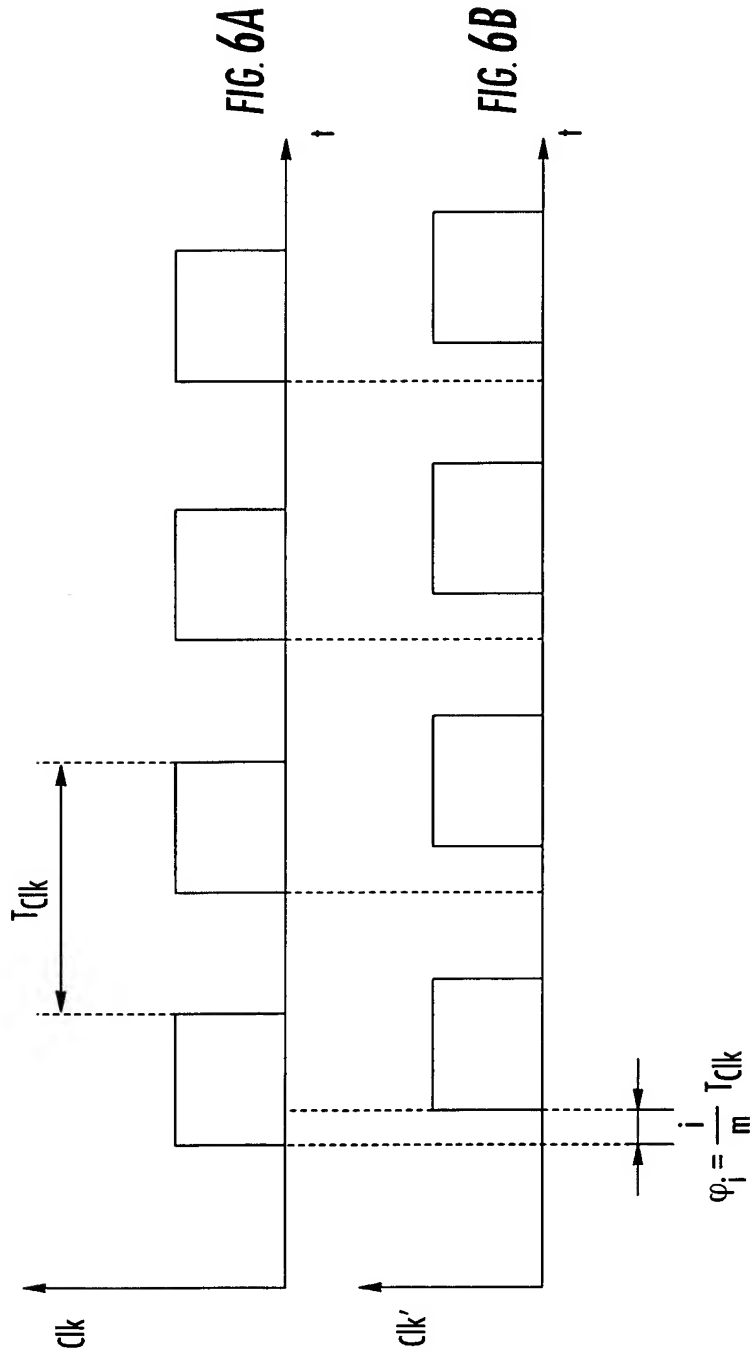
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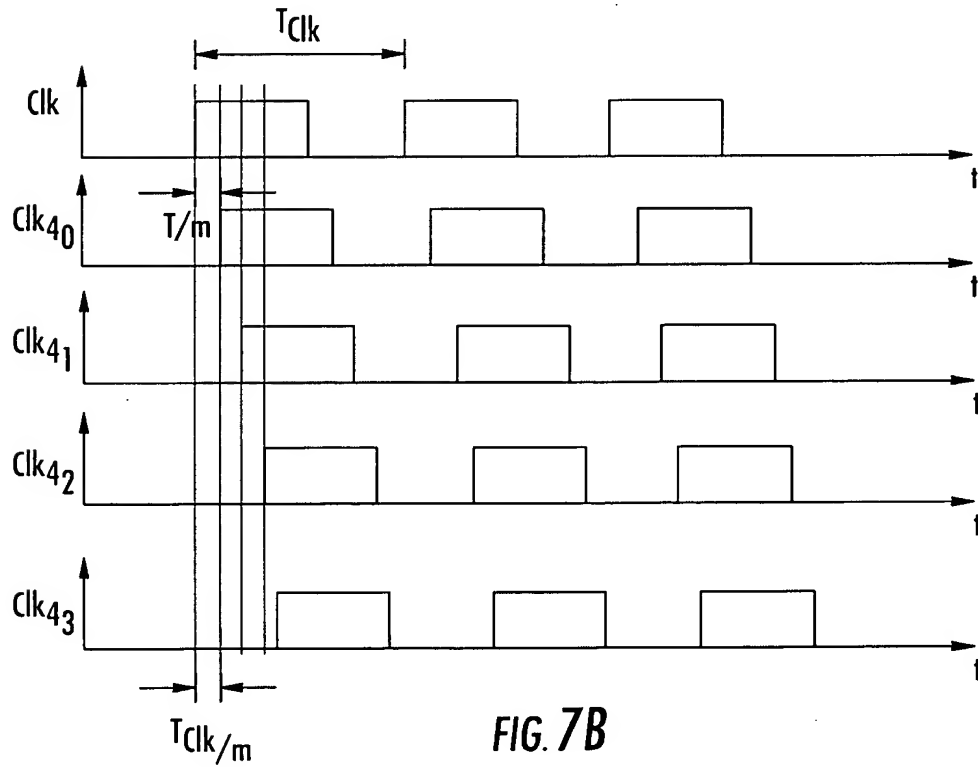
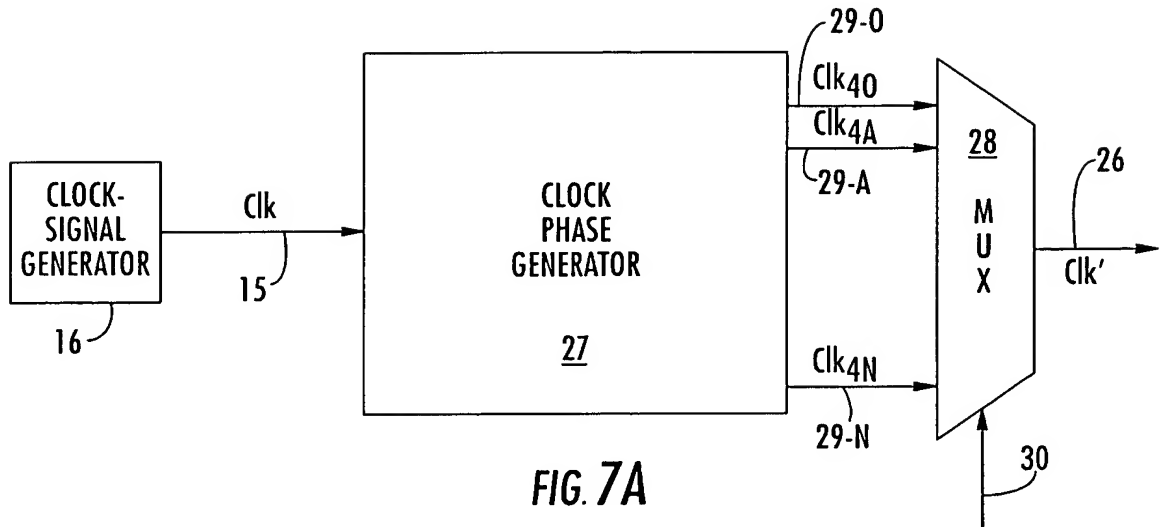
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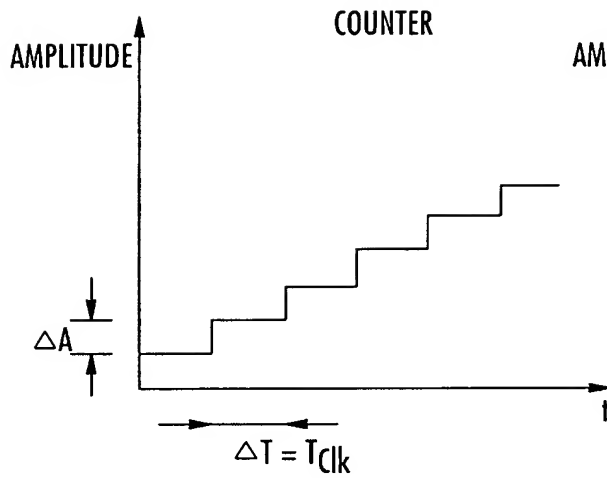


FIG. 8A

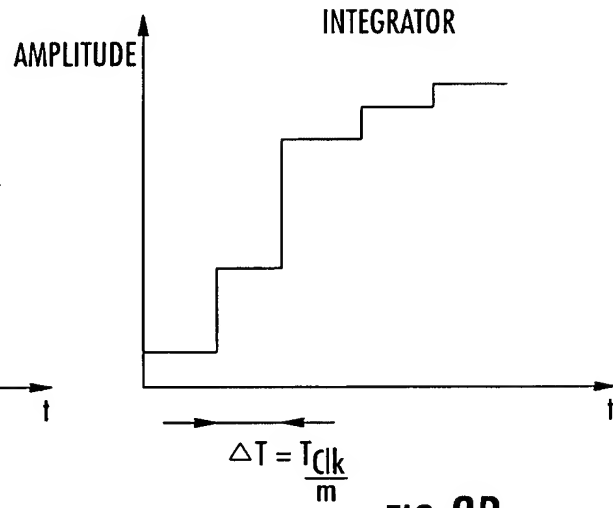


FIG. 8B

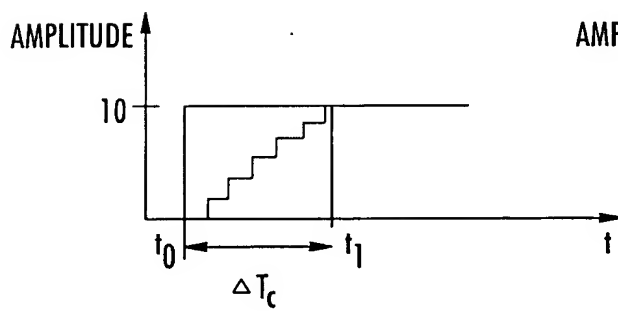


FIG. 9A

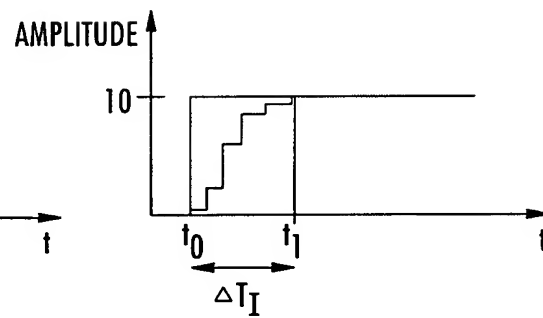


FIG. 9B

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The diagram shows the timing of a memory buffer system. The vertical axis represents TIME, and the horizontal axis represents DISTANCE FROM MEMORY BUFFER. The diagram includes a vertical line for the MEMORY BUFFER, a vertical line for MM4, and a vertical line for MM0. The horizontal axis is marked with points 1, 2, 3, 4, 5, 6, and 7. The time interval between points 2 and 3 is labeled t_{23} . The diagram shows that the distance from the memory buffer to MM4 is constant for components 1, 2, 3, and 4, and increases linearly for components 5 and 6. The distance from the memory buffer to MM0 is constant for components 1, 2, 3, and 4, and increases linearly for components 5 and 6.

FIG. 10

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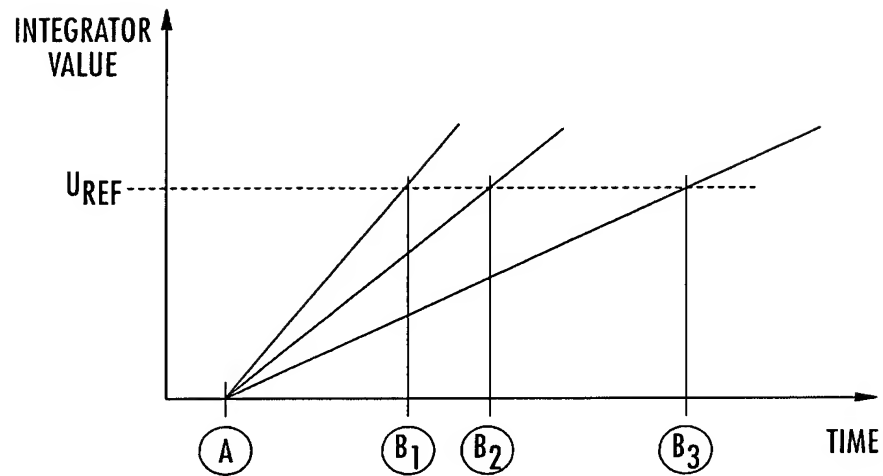


FIG. 11

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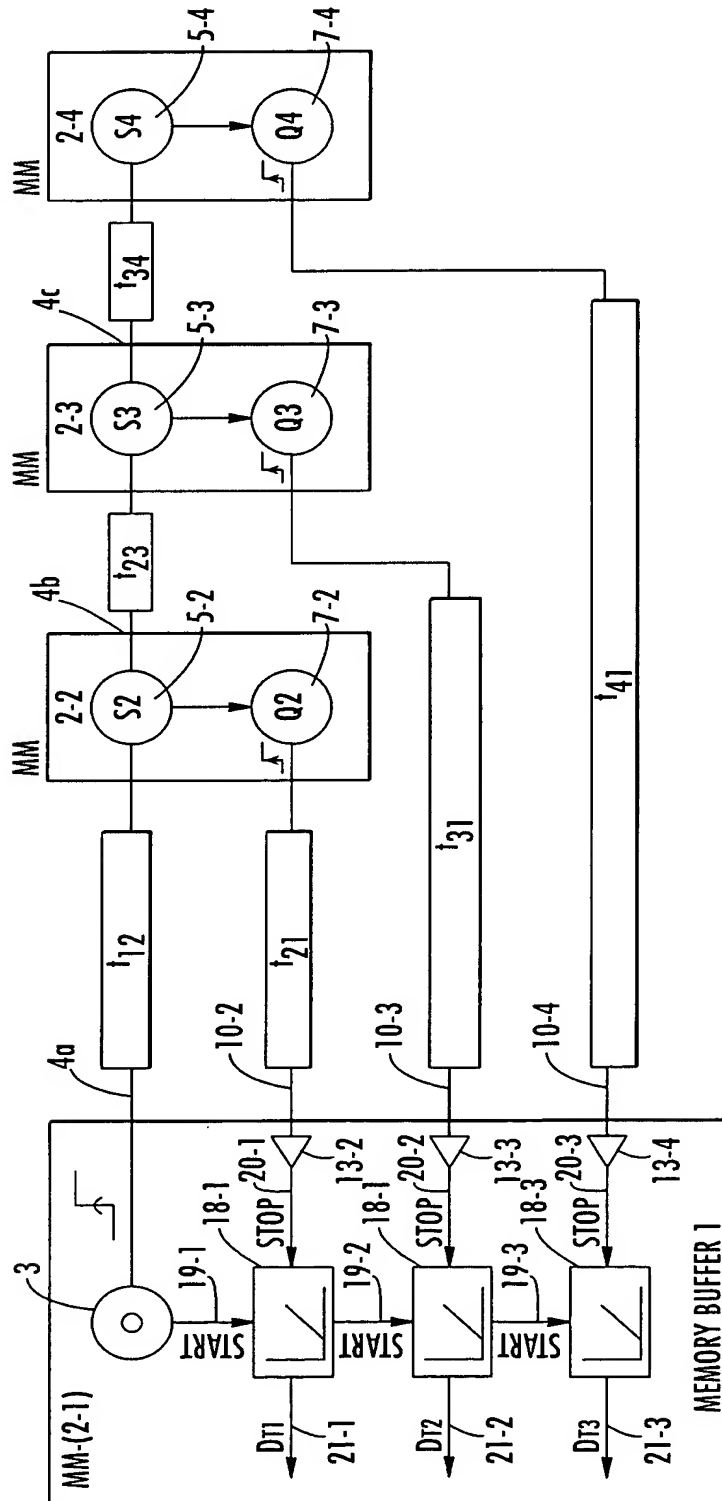


FIG. 12

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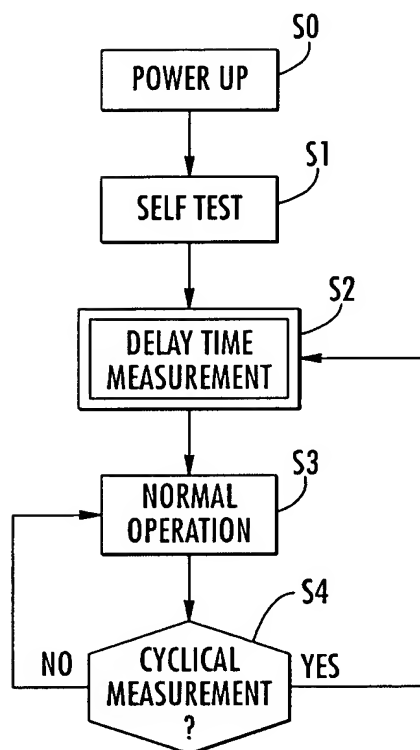


FIG. 13